A COMBINED MMIC/MIC 8-CHANNEL RECEIVE ONLY PHASED ARRAY DEMONSTRATOR OPERATING IN I/J BAND

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ABSTRACT

An eight element phased array receiver operating in I/J band is presented. Both MMIC and MIC technologies are employed. Chip yield, electronic control, basic system operation and engineering configuration are discussed.

INTRODUCTION

The work detailed in this paper describes the design of an eight element/channel receive only phased array demonstrator operating in I/J band, utilising both MMIC and MIC components.

The MMIC devices were developed in close collaboration with GEC's Hirst Research Centre, Wembley, England. A foundry approach for design, re-design and associated chip manufacture has been pursued.

Objectives in the work were to achieve basic electronic beam scanning, but more importantly, to assess the GaAs technology base available to a Systems Company. A constraint of approximately 80 mm diameter for the physical build of the unit was targetted. Chip yield and cost would have to see accurate address, with yield itself also taking into account 'acceptable performance' as a criteria for overall yield.

DEMONSTRATOR CONFIGURATION

The demonstrator consists of four sub-assemblies; Antenna, RF Channel(s), Local Oscillator Unit and IF Combiner/supply and Logic Interface.

The IF combiner board and supply and logic interface PCBs are housed away from the main RF assemblies (connected via IF and DC cables) for reasons of cost and general convenience during array assessment. This approach also allows individual RF channels to be bench tested prior to final array investigation.

ANTENNA ARRAY

A planar eight element patch antenna fabricated on Duroid dielectric constant, Er = 2.2, and 1.6 mm thick, forms the design (1). The patches, which behave as half wave microstrip resonators, are fed via co-axial lines through the ground plane to the 50 ohm point of the patch. Design centre frequency for the array is 10.5 GHz with a nominal bandwidth of 5%.

The array produces linear polarisation with a predicted gain of 13 dBiL. The theoretical 3 dB beamwidth is 30 degrees, with beam scanning out to +/- 50 degrees. Measurements to date exhibit a nominally 4% bandwidth centred on 10.5 GHz, with an associated 8 dB of return loss. Single element gain is 7.2 dBiL, 1 dB lower than predicted. Cross polar content is better than 8 dB across the stated beam scanning range. Sum pattern total beamwidth, obtained using 4 of the patches is 24 degrees. A photograph of the manufactured array is shown in Fig 1.

RF CHANNEL

A total of eight RF channels are employed, each of which receives an RF signal from its respective patch, located on the planar antenna array. Each channel is identical in both its mechanical and electrical construction. The channel performs as a conventional superheterodyne receiver with the addition of phase control in the local oscillator signal path, thereby shifting the phase of the IF waveform. A 4-bit time delay phase shifter is used, offering discrete 22.5 degree increments from 0 to 360 degrees. The IF frequency to be used is 50 MHz.

A circuit diagram of the RF channel is shown in Fig 2.

Components detailed in the receiver are now briefly described.

MIXER

This device is of a single balanced

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Schottky barrier diode configuration (2). RF and LO signals are fed into two arms of a Lange coupler, which in turn feeds the necessary phase shifting and matching circuitry. Output filtering provides a DC to 500 MHz IF bandwidth. The measured conversion loss of the mixer is typically 6 dB, for an LO drive level of +10 dBm.

PHASE SHIFTER - 4-BIT

This design employs a Lange coupler whose two arms (ports 2 and 3) are individually loaded with a transmission line on which are placed shunt mounted Schottky diodes (3). A total of 32 diodes are used, with pairs of diodes being switched in relation to the phase state required. The reverse bias capacitance of the diodes in the off state is used as part of an artificial transmission line, the inductive elements being provided by lengths of transmission line.

RF AMPLIFIER

The primary function of this amplifier is to negate the losses in the local oscillator signal path, such that a +7 to +10 dBm power level is incident on the mixer. This power level will yield a conversion loss of between 6 and 7 dB typically. Note that in Fig 2 a pre-amplifier is shown in the RF line before the mixer. This device will be the same RF amplifier as used in the LO line. Its function is purely as demonstration of a pre-mixer gain stage. The amplifier under development is being designed as a general purpose gain block employing 1 micron gate features, and is therefore, not designed for a low noise figure. RF channels are being constructed with and without this pre-amplifier to assess mixer sensitivity when used in the system.

Target performance for the amplifier is +10 dB gain at 10.5 GHz with a +10 dBm minimum saturated output power.

Amplifier measurements to date show gain figures of between 7.6 - 9.8 dB at 10.5 GHz, and saturated output powers in excess of + 10 dBm.

IF AMPLIFIER

This device is a bought-in 'Avantek' silicon MMIC module, exhibiting 18-20 dB of gain at 50 MHz. It is small in size and ideal for surface mounting on standard MIC substrate material.

LOCAL OSCILLATOR UNIT

The local oscillator signals required by each of the eight RF channels are supplied from a single FET based DRO MIC, with varactor tuning (4). Oscillator output is fed via a Lange coupler feeding two MMIC amplifiers (as previously mentioned) into two MIC distributed 4-way power splitters (5). These circuit elements are contained within a single mechanical package with all 8 RF outputs being closely phase and amplitude matched at the operational frequency. The unused port of the Lange coupler will be used for monitoring the oscillator frequency, thus allowing adjustment of the oscillator with the incoming RF signal during test maintaining the 50 MHz IF required. Fig 3 shows the Local Oscillator circuit diagram. Measured oscillator performance shows an initial tuning range of 10.364 to 10.509 GHz (145 MHz) with an associated +16.4 dBm to +17.9 dBm of output power. Typical 1 MHz side band level is -48 dBc.

A photograph of the Local Oscillator unit is depicted in Fig 4.

BEAM FORMING AND PHASE SHIFTER CONTROL

The eight discrete antenna element patterns are summed together into four pairs which theoretically reduces the system to a four element array. Beam forming is achieved by phase shifting each of the element pairs. Phase settings for the individual element pairs (ie phase shifter settings in each RF channel) have been calculated for various beam scan angles in the azimuth plane.

Phase shifter control, which requires forward biasing of a pair of Schottky diodes in each phase shifter, is via EPROMS. For demonstration purposes, stepped beam angles of ten degrees are used.

The sum and difference target information is extracted in the IF combiner board, which is essentially several 50 MHz lumped element power combining circuits, followed by detector diodes.

MECHANICAL CONSIDERATIONS

The requirements on the mechanical front were to be that each part of the array demonstrator could be individually tested prior to final assembly, and that interchangeability or part replacement would prove a simple task. As a result, the RF channels are mechanically identical, which also minimises manufacturing and design costs.

RF CHIP INTERCONNECT

Individual GaAs chips are mounted onto metal carriers, which also support the alumina feed tiles. Chips on carriers are then checked for functionality after the assembly stage. Final chip/carrier integration into the RF modules then takes place. A CAD plot of the MIC tile used is shown in Fig 5.

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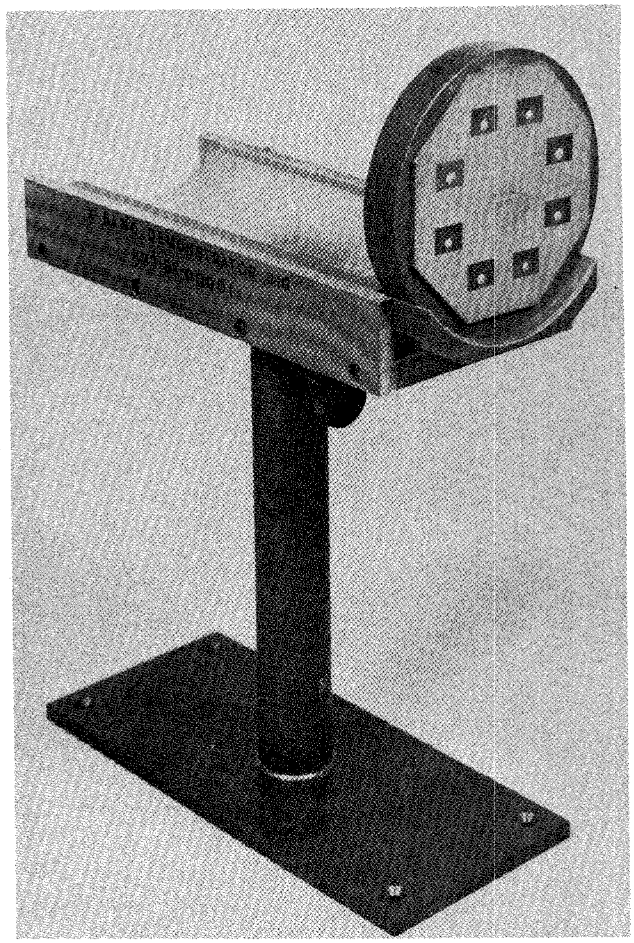

Fig 1. Antenna Array

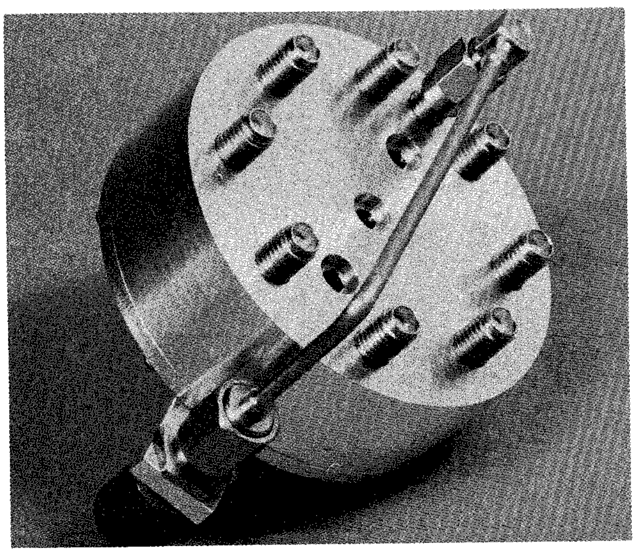

Fig 4. Local Oscillator Unit

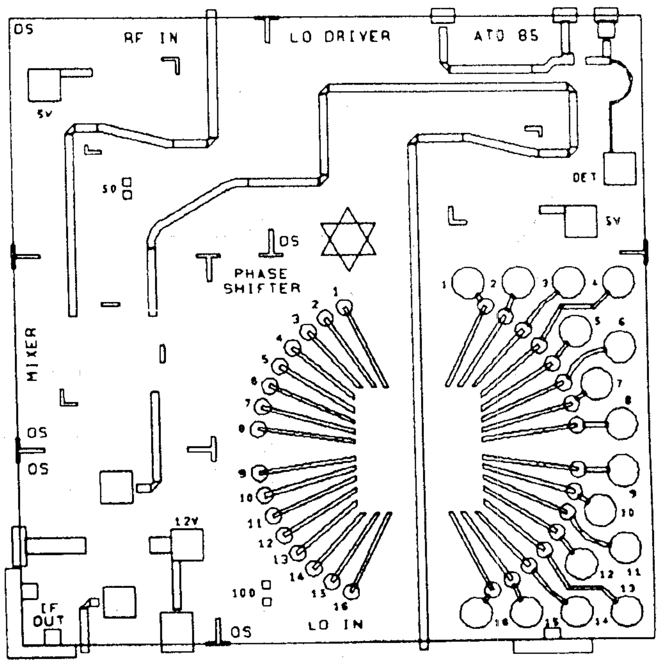

Fig 5. MIC CAD Layout

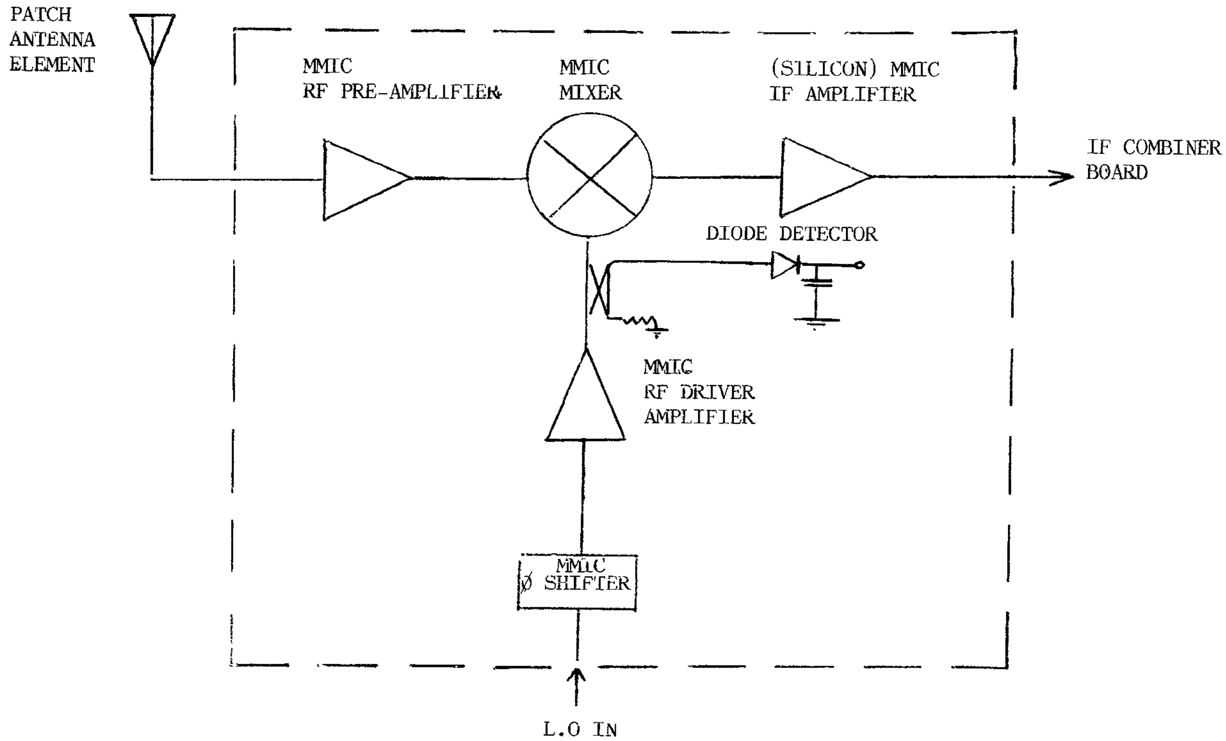

Fig 2. RF Channel Block Schematic

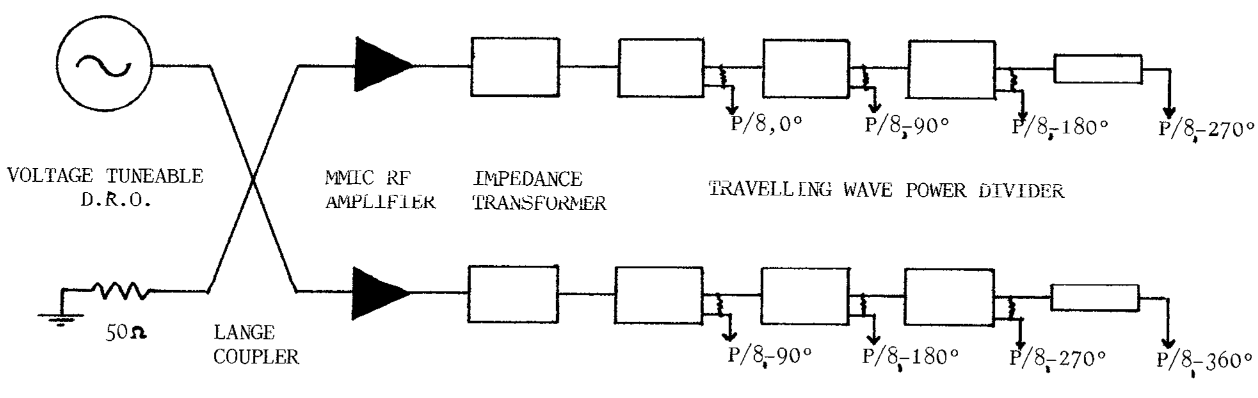

Fig 3. Local Oscillator Unit Block Schematic